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1. A semicustom integrated circuit comprising:

(a) a plurality of cell rows, in each row a plurality of standard cell are arranged, the standard cells being configured as rectangular pattern regions having a predetermined height, and different widths so that the standard cells include first and second type cells; and

(b) gate array basic cells formed in an empty space of a predetermined cell row of the plurality of cells rows, each of the basic cells being configured as a rectangular pattern region having a height substantially identical to said predetermined height and a width equal to the width of the first type cell, said width of the basic cells not being equal to the width of the second type cell.

2. The integrated circuit of claim 1, wherein the basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

3. The integrated circuit of claim 1, further comprising;

gate array basic cells formed in wiring channel regions disposed between the plurality of cell rows.

4. The integrated circuit of claim 1, wherein respective cell rows are arranged adjacently.

5. The integrated circuit of claim 3, wherein the basic calls formed in the wiring channel regions are formed on a basis of a rectangular pattern having a height substantially identical to that of the standard cells.

6. The integrated circuit of claim 3, wherein the standard cells and the basic cells are arranged adjacently along a direction orthogonal to the cell rows.

7. The integrated circuit of claim 4, wherein the standard cells and the basic cells are arranged adjacently along a direction orthogonal to the cell rows.

8. The integrated circuit of claim 3, wherein the standard cells and the basic cells which are arranged adjacently along a direction orthogonal to the cell rows have common signal lines.

9. The integrated circuit of claim 4, wherein the standard cells and the basic cells which are arranged adjacently along a direction orthogonal to the cell rows have common signal lines.

10. The integrated circuit of claim 1, wherein the standard cells and the basic cells have common power supply lines arranged along a straight line.

11. The integrated circuit of claim 1, wherein the standard cells and the basic cells have common signal lines arranged along a straight line.

12. The integrated circuit of claim 1, wherein widths of the standard cells are integral multiple of a width of the basic cells.

13. The integrated circuit of claim 5, wherein widths of the standard cells are integral multiple of a width of the basic cells.

14. The integrated circuit of claim 1, wherein the standard cells and the basic cells are arranged pursuant to a same grid system.

15. The integrated circuit of claim 3, wherein the standard cells and the basic cells are arranged pursuant to a same grid system.

16. The integrated circuit of claim 1, wherein the basic cells are used to construct intermediate buffers for distributing a clock signal to a plurality of circuits which are displaced on a semiconductor substrate.

17. The integrated circuit of claim 3, wherein the basic cells are used to construct intermediate buffers for distrib-

uting a clock signal to a plurality of circuits which are displaced on a semiconductor substrate.

18. The integrated circuit of claim 3, wherein the basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

19. A semicustom integrated circuit having a logic circuit area and at least one of megacell and megafunction on a single semiconductor chip, the logic circuit area comprising:

(a) a plurality of cell rows, in each row a plurality of standard cells are arranged, the standard cells being configured as rectangular pattern regions having a predetermined height, and different widths so that the standard cells include first and second type cells; and

(b) gate array basic cells formed in an empty space of the standard cells in predetermined cell row of the plurality of cell rows, each of the basic cells being configured as a rectangular pattern region having a height substantially identical to said predetermined height and a width equal to the width of the first type cell, said width of the basic cells not being equal to the width of the second type cell.

20. The integrated circuit of claim 19, further comprising:

gate array basic cells formed in wiring channel regions between the plurality of cell rows.

21. The integrated circuit of claim 10, wherein the standard cells and the basic cells are arranged pursuant to a same grid system.

(Reissue Claim 22) The integrated circuit of claim 1, wherein each gate array basic cell has the same pattern of gate electrodes and the same pattern of impurity regions.

(Reissue Claim 23) The integrated circuit of claim 1, wherein said standard cells include a third type cell having a width different from the widths of the first type cell and the second type cell.

(Reissue Claim 24) The integrated circuit of claim 19, wherein each gate array basic cell has the same pattern of gate electrodes and the same pattern of impurity regions.

(Reissue Claim 25) The integrated circuit of claim 19, wherein said standard cells include a third type cell having a width different from the widths of the first type cell and the second type cell.

(Reissue Claim 26) The integrated circuit of claim 19, wherein the basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

(Reissue Claim 27) The integrated circuit of claim 19, wherein respective cell rows are arranged adjacently.

(Reissue Claim 28) The integrated circuit of claim 19, wherein the standard cells and the basic cells have common power supply lines arranged along a straight line.

(Reissue Claim 29) The integrated circuit of claim 19, wherein widths of the standard cells are integral multiple of a width of the basic cells.

(Reissue Claim 30) A semiconductor integrated circuit comprising:

a plurality of standard cells arranged in each of a plurality of adjacent cell rows, said plurality of standard cells in each row having at least two different widths; and

a plurality of gate array basic cells arranged in said cell rows in which said standard cells are arranged, each gate array basic cell having the same pattern of gate electrodes and the same pattern of impurity regions so that a width of each gate array basic cell is equal to each other,

wherein said width of each gate array basic cell is substantially identical to a first one of the at least two different widths of said standard cells.

(Reissue Claim 31) The integrated circuit of claim 30, wherein the plurality of standard cells have at least three different widths.

(Reissue Claim 32) The integrated circuit of claim 30, wherein a second one of the at least two different widths of said standard cells is substantially identical to an integral multiple of said width of said gate array basic cell.

(Reissue Claim 33) The integrated circuit of claim 30, wherein in each row, a first impurity diffusion region and a second impurity diffusion region are arranged in the direction of said cell rows, said standard cells and gate array basic cells being arranged in said first and second impurity diffusion regions.

(Reissue Claim 34) The integrated circuit of claim 33, wherein said first and second impurity diffusion regions are well regions.

(Reissue Claim 35) The integrated circuit of claim 33, wherein each cell row has a first row and a second row adjacent to each other, in each cell row the first impurity diffusion region is arranged in one of the first and second rows and the second impurity diffusion region is arranged in the other of the first and second rows.

(Reissue Claim 36) The integrated circuit of claim 35, wherein at least one cell row has the first impurity diffusion region in the first row, and at least one cell row has the first impurity diffusion region in the second row.

(Reissue Claim 37) The integrated circuit of claim 35, further comprising power supply wirings for supplying power to said standard cells and gate array basic cells, disposed above said adjacency of said first and second rows.

(Reissue Claim 38) The integrated circuit of claim 37, wherein said power supply wirings are made of a first-metal wiring layer.

(Reissue Claim 39) The integrated circuit of claim 38, wherein said standard cells and said gate array basic cells are wired by wirings made of at least said first-metal wiring layer, second and third-metal wiring layers disposed above said first-metal wiring layer in order.

(Reissue Claim 40) The integrated circuit of claim 39, wherein a width of said power supply wirings is at least twice as wide as a width of said wirings.

(Reissue Claim 41) The integrated circuit of claim 38, wherein said wirings made of said first and second-metal wiring layer are disposed in direction parallel to said cell rows, and said wirings made of said third-metal wiring layer are disposed in direction perpendicular to said cell rows.

(Reissue Claim 42) The integrated circuit of claim 33, wherein each of said first and second impurity diffusion regions has a contact region of the same impurity type therein, wherein an impurity concentration of said contact region is higher than in of each of the first and second impurity diffusion regions.

(Reissue Claim 43) The integrated circuit of claim 30, wherein the gate array basic cells are used to construct intermediate buffers for distributing a clock signal to a plurality of circuits which are displaced on a semiconductor substrate.

(Reissue Claim 44) The integrated circuit of claim 30, wherein the gate array cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

(Reissue Claim 45) The integrated circuit of claim 30, further comprising at least one of megacell and megafunction in another area of a plurality of cell rows on a single semiconductor chip.

(Reissue Claim 46) The integrated circuit of claim 45, wherein said megacell is one of ROM or RAM or both, and said megafunction is one of ALU or CPU or both.

(Reissue Claim 47) A semiconductor integrated circuit having a logic circuit area and at least one of megacell and megafunction on a single semiconductor chip, the logic circuit area comprising:

a plurality of standard cells arranged in each of a plurality of adjacent cell rows, said plurality of standard cells in each row having at least two different widths; and

a plurality of gate array basic cells arranged in said cell rows in which said standard cells are arranged, each gate array basic cell having the same pattern of gate electrode and the same pattern of impunity regions,

wherein said width of each gate array basic cell is substantially identical to a first one of the at least two different widths of said standard cells.

(Reissue Claim 48) The integrated circuit of claim 47, wherein a second one of the at least two different widths of said standard cells is substantially identical to an integral multiple of said width of said gate array basic cell.

(Reissue Claim 49) The integrated circuit of claim 48, wherein a height of said standard cells is substantially identical to a height of said gate array basic cells.

(Reissue Claim 50) The integrated circuit of claim 47, wherein each row, a first impurity diffusion region and a second impurity diffusion region are arranged in the direction of said cell rows, said standard cells and gate array basic cells being arranged in said first and second impurity diffusion regions.

(Reissue Claim 51) The integrated circuit of claim 50, wherein said first and second impurity diffusion regions are well regions.

(Reissue Claim 52) The integrated circuit of claim 50, wherein each cell row has a first row and a second row adjacent to each other, in each cell row the first impurity diffusion region is arranged in one of the first and second rows and the second impurity diffusion region is arranged in the other of the first and second rows.

(Reissue Claim 53) The integrated circuit according to claim 52, wherein at least one cell row has the first impurity diffusion regions in the first row, and at least one cell row has first the impurity diffusion region in the second row.

(Reissue Claim 54) The integrated circuit of claim 50, further comprising power supply wirings for supplying power to said standard cells and gate array basic cells, disposed above said adjacency of said first and second rows.

(Reissue Claim 55) The integrated circuit of claim 54, wherein said power supply wirings are made of first-metal wiring layer.

(Reissue Claim 56) The integrated circuit of claim 55, wherein said standard cells and said gate array basic cells are wired by wirings made of at least said first-metal wiring layer, second and third-metal wiring layer disposed above said first-metal wiring layer in order.

(Reissue Claim 57) The integrated circuit of claim 56, wherein a width of said power supply wirings is at least twice as wide as a width of said wirings.

(Reissue Claim 58) The integrated circuit of claim 56, wherein said wirings made of said first and second-metal wiring layer are disposed in direction parallel to said cell rows, and said wirings made of said third-metal wiring layer are disposed in direction perpendicular to said cell rows.

(Reissue Claim 59) The integrated circuit of claim 50, wherein each said first and second diffusion regions has contact region of the same impurity type therein, wherein an impurity concentration of said contact region is higher than it of each diffusion regions.

(Reissue Claim 60) The integrated circuit of claim 47, wherein the gate array basic cells are used to construct intermediate buffers for distributing a clock signal to a plurality of circuits which are displaced on a semiconductor substrate.

(Reissue Claim 61) The integrated circuit of claim 47, wherein the gate array basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

(Reissue Claim 62) The integrated circuit of claim 47, wherein said megacell is one of ROM or RAM or both, and said megafunction is one of ALU or CPU or both.

(Reissue Claim 63) The integrated circuit of claim 47, wherein said standard cells and said gate array basic cells are arranged over substantial entire region of each said cell rows, edges of each said cell rows are in straight line.

(Reissue Claim 64) The integrated circuit of claim 63, wherein said at least one of megacell and megafunction has a rectangular pattern, edges of each said cell rows of and one side of said rectangular pattern are in straight line.

(Reissue Claim 65) The integrated circuit of claim 47, wherein the plurality of standard cells have at least three different widths.